

## Electronic Acknowledgement Receipt

<b>EFS ID:</b>	3012743
<b>Application Number:</b>	10783589
<b>International Application Number:</b>	
<b>Confirmation Number:</b>	1594
<b>Title of Invention:</b>	Regulating unused/inactive resources in programmable logic devices for static power reduction
<b>First Named Inventor/Applicant Name:</b>	Kevin T. Look
<b>Customer Number:</b>	24309
<b>Filer:</b>	Justin Liu/Katherine Stofer
<b>Filer Authorized By:</b>	Justin Liu
<b>Attorney Docket Number:</b>	X-1462-2P US
<b>Receipt Date:</b>	17-MAR-2008
<b>Filing Date:</b>	20-FEB-2004
<b>Time Stamp:</b>	22:00:29
<b>Application Type:</b>	Utility under 35 USC 111(a)

### Payment information:

Submitted with Payment	no
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### File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement Letter	X1462_2P_US_Sup_IDS_efiled.pdf	51048 49a2708b382c3ef78c3cfa62073994ca84868830	no	1

### Warnings:

### Information:

2	NPL Documents	Allen_Holberg_Bandgap_Voltage_NPL.pdf	65302	no	5
			47896f081834d81277e1d6135909ce999c599b02		
Warnings:					
Information:					
3	NPL Documents	Intel_PXA27X_Proc_Fam_Pwr_Req_AppNote_2004_NPL.pdf	583969	no	36
			5f9e6404270e7e2cb03737534591103c01b41a26		
Warnings:					
Information:					
4	NPL Documents	Microchip_Tech_Micropower_Voltage_NPL.pdf	698019	no	28
			d02ddfd71492e04a17e93e0799b8ef0bc9f0a927		
Warnings:					
Information:					
5	NPL Documents	Nowka_et al_A_32_bit_PowerPC_NPL.pdf	552946	no	7
			2e7741beb62a66aa40cdd2e26890de242fa106b		
Warnings:					
Information:					
6	NPL Documents	Texas_Instruments_DS_BQ4011_05_99_NPL.pdf	373289	no	15
			dc8b7404b80cde6d34f904cac7d110c1347d8bcb		
Warnings:					
Information:					
7	NPL Documents	Texas_Instruments_DS_BQ4011_08_93_NPL.pdf	235384	no	11
			3e099e8f2e564e886098ea3c781b6462a2082ecd		
Warnings:					
Information:					
8	NPL Documents	Xilinx_DS313_Spartan_3L_Low_Power_FPGA_NPL.pdf	377709	no	10
			edbcbbddf9f7c94584bafbd4dca824e6b040a9b1a6		
Warnings:					
Information:					
9	NPL Documents	Virtex_Two_Pro_FPGA_NPL.pdf	2803551	no	56
			f5ea680e1c4aab9614e3e46bd522b10a9420489c		
Warnings:					
Information:					
10	Information Disclosure Statement (IDS) Filed	X1462_2P_US_SB08A_efiled.pdf	112847	no	4
			8ca21f187c72eb5b79279c20c6de82a9eca41f10		
Warnings:					
Information:					

**Total Files Size (in bytes):**

5854064

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**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**